OPERATING MANUAL

MODEL 5101

FREQUENCY SYNTHESIZER CHANNEL

WAVETEK

WAVETEK SAN DIEGO, INC.

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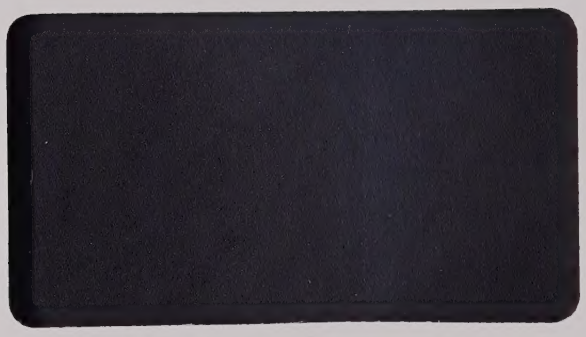

OPERATING MANUAL

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FREQUENCY SYNTHESIZER CHANNEL

Part No. 800.3161

WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warrantied within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

Wavetek shall have no responsibility hereunder for any defect or damage caused by improper storage, improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, accident or for any product which has been repaired or altered by anyone other than Wavetek or its authorized representative and not in accordance with instructions furnished by Wavetek.

Exclusion of Other Warranties

The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.**

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

The Model 5101 Frequency Synthesizer Channel generates spectrally pure and stable output frequencies from 1 Hz to 3 MHz with constant 1 Hz resolution. It utilizes a unique direct digital synthesis technique* to generate the output sinusoid. Complementary TTL compatible square wave outputs are provided for monitoring the output of the channel.

The Model 5101 Frequency Synthesizer Channel is used primarily in the Rockland Systems Corporation System 51. The System 51 is a multi-channel Frequency Synthesizer System (up to 48 channels) designed for ease of operation, is virtually maintenance free, at very reasonable cost. The Model 5101 Frequency Synthesizer Channel obtains its input power, clock, control logic, and programming information from the System 51. The purpose of this manual is to supply the necessary information to operate the Model 5101 Frequency Synthesizer Channel as a stand-alone assembly.

1-2. THEORY OF OPERATION

The Model 5101 utilizes direct digital synthesis techniques to generate the output sinusoid. Samples of the sinusoid are digitally generated at an 8 MHz rate and are then converted to analog form by a digital-to-analog converter (DAC) and a smoothing low pass filter which cuts off at approximately 3.5 MHz. The amplitude of the digital samples is represented by 11 bits (including sign). A block diagram of the Model 5101 is given in Figure 1. The frequency stability and accuracy of the output sinusoid is related directly to the system clock.

The frequency of the output signal is stored in a frequency register which can, on command, transmit its programmed data back over the 22 programming lines. The register stores the frequency in a modified binary form, with both 3-decade groups (Hz and KHz) represented by separate 10-bit word. The two MHz bits appear as two bits on the most significant end of the KHz word, making it 12 bits in length. This data is presented to a phase accumulator whose rate of phase accumulation is directly proportional to its input. The phase accumulator output is a linearly increasing binary equivalent of $0\text{-}90^0$. A read-only-memory (ROM) has programmed in it the appropriate sine function value for each phase angle address. By proper use of data complementing at the input and output of the ROM, the entire sinusoidal cycle can be produced.

*U.S. Patent No. 3,735,269

1-2. THEORY OF OPERATION - continued

The output of the ROM, which is now an 11-bit binary word, is converted to staircase-waveform approximation of a sinusoid by a digital-to-analog converter (DAC). The low pass filter smooths the sinusoid to the rated spectral purity. Since 11 bits of phase resolution are used, the phase accuracy of each converted sample deviates no more than $\pm 0.09^0$ from a pure sinusoid. The low pass filter output is then fed to an output amplifier. The two sinusoidal outputs are driven by the amplifier. A squaring circuit also derives its input from this point, and provides two complementary TTL-compatible outputs.

Also contained within the Model 5101 Synthesizer is the control logic which interfaces the synthesis and program load/read facilities.

1-3. SPECIFICATIONS

Output Frequency Range: 1 Hz to 2,999,999 Hz

Frequency Resolution: 1 Hz throughout entire range

Output Signals:

Sinewave Output #1: Fixed amplitude, 1 volt RMS with 50-ohm source impedance (Any fixed level up to 3 volts RMS at 50 ohms available on request)

Spurious Components: (see CAUTION below) Harmonic components do not exceed -40 dB. Non-harmonic components typically do not exceed -50 dB from 1 Hz and -40dB from 2 Mhz to 3 MHz; -45 dB at 1.5 MHz ±10 Hz.

Phase Noise: (see CAUTION below) Phase noise in 30 KHz band excluding 1 Hz centered on carrier does not exceed -50 dB from 1 Hz to 2 MHz and -40 dB from 2 MHz to 3 MHz.

Square Wave Output #2: TTL level capable of driving 30 standard TTL loads. Same phase noise specification as Output #1.

Square Wave Output #3: TTL level capable of driving 30 standard TTL loads, complementary to Output #2. Same phase noise specification as Output #1.

Frequency Control: Output frequency may be selected via a 22-bit parallel binary word, and the programmed frequency may be read out over the same bus.

Programming Delay: 2 μsec max with amplitude and phase continuity maintained between any two programmed frequencies.

Update Rate: Programmed frequencies may be updated at 0.125 μsec intervals.

Input Signals: Requires 8 MHz Reference Oscillator Clock (TTL). Input loading is one standard TTL load.

1-3. SPECIFICATIONS - continued

Input Power: Requires regulated +5VDC at 2.5 Amps and ±15VDC at 100 mA.

Temperature: 0°C to +50°C operating, -20°C to +70°C non-operating.

Dimensions: 8.75" high x 1.35" wide x 15" deep.

Mating Connectors: Programming mating connectors: Amphenol #205514-1
TTL outputs: Viking GP3-4CE-26.

C A U T I O N

The specifications on spectral purity (spurious components and phase noise) are applicable when Model 5101 Frequency Synthesizer Channel is contained in the System 51 where adequate shielding, crystal reference input, power supplies and programming lines have been provided.

Proper arrangements must be made to assure sufficient air flow around and through Model 5101 when it is mounted in its enclosure.

SECTION II

OPERATION

2-1. INTRODUCTION

The Model 5101 Frequency Synthesizer Channel when used as a stand-alone assembly requires power, an 8 MHz reference clock, programming data and control signals.

2-2. INTERFACE DESCRIPTION

A description of the programming connector can be found in Table 1. The following is a description of this interface:

2-2-1. Power: +5VDC at 2.5 amps; ±15VDC at 100 mA.

2-2-2. Input Reference: 8 MHz Reference Clock, TTL, duty cycle approximately 50%. It is recommended that this input be transmitted via coax cable. The frequency limits of this signal are from DC to 8.1 MHz. The deviation of the frequency of the output signal (the programmed frequency) is directly proportional to the deviation of the external clock from 8 MHz. Operation at frequencies below 8 MHz results in a lower sampling rate; the internal low pass filter which removes sampling components from the output signal is designed for an 8 MHz sampling rate and becomes less effective as the sampling rate is lowered. To maintain full harmonic and spurious distortion specifications, an external low pass filter is required to eliminate these components. Cutoff frequency of this filter should be slightly above highest output frequency.

2-2-3. Programming Data (A0 to A21): The frequency programming lines are bidirectional. The Model 5101 frequency programming interface is a tri-state TTL bus and should be driven with open collector or tri-state devices. To program a given frequency, verify proper logic states of the control lines (2-2-4). The weight of each program line is shown in Table 1. Positive logic is used: a logical "1" on any line will cause a contribution to the frequency equal to the weight of that line. Any binary number less or equal to 999_{10} = $11111\ 00\ 111_2$ is valid for each of the two frequency ranges (Hz and KHz). When the Model 5101 Frequency Synthesizer Channel is interrogated (refer to 2-2-4 for the appropriate logic levels on the control lines), the stored programmed information is transmitted over the programming lines. A logic "1" indicates a contribution equal to the weight of the line.

2-2. INTERFACE DESCRIPTION - continued

2-2-4. Control Lines

Enable - low active - when more than one Model 5101 is used in a system, this line allows selection of a specific unit for participation in loading and reading frequency commands from a common control bus. Only one unit should be enabled at any time. When the Model 5101 is used as a stand-alone synthesizer, this line could be tied to ground. A logic "0" on this line is required in order to load frequency data or to read stored frequency data.

Read - low active - a logic "0" on this line allows the Model 5101 to transmit the programmed frequency over the frequency programming lines (provided the enable line is low). If the Model 5101 is not to be interrogated, this line should be held high.

Load - low active - a logic "0" on this line allows the Model 5101 to be programmed to the frequency information contained on the programming lines (provided the enable line is low).

NOTE: The Read and Load lines should NOT be held low simultaneously.

2-2-5. Status Lines

Acknowledge - low active - transmitted on a tri-state bus. A logic "0" indicates the Model 5101 Frequency Synthesizer Channel has been enabled and a frequency was loaded.

Presence - low active - transmitted on a tri-state bus. A logic "0" indicates the Model 5101 Frequency Synthesizer Channel has been enabled.

2-2-6. Test Points

Hz Carry - test point for verification of proper operation of the accumulator section. Should be left open.

KHz Carry - test point for verification of proper operation of the accumulator section. Should be left open.

Sign Bit - test point. Should be left open.

2-3. EXAMPLE OF MODEL 5101 PROGRAMMING

To program the Model 5101 to 2,500,010 Hz, the following must be performed:

1. Supply +5VDC, +15VDC and -15VDC as per Table 1.

2. Supply a 8 MHz clock as per Table 1.

3. Leave the Hz Carry, KHz Carry, Zero Phase lines open.

4. Set the Enable line to a logic "0" (low). (The presence line will go to logic "0")

5. Set the Read line to a logic "1" (high).

6. Set the following lines to a logic "1": 2 MHz (pin M), 256 KHz (pin $\bar{A}$), 128 KHz (pin $\bar{E}$), 64 KHz (pin $\bar{K}$), 32 KHz (pin $\bar{H}$), 16 KHz (pin C), 4 KHz (pin U), 8 KHz (pin $\bar{D}$), and 2 Hz (pin V).

7. Set the following lines to a logic "0": 1 MHz (pin S), 512 KHz (pin W), 512 Hz (pin T), 256 Hz (pin X), 128 Hz (pin $\bar{B}$), 64 Hz (pin $\bar{F}$), 32 Hz (pin $\bar{M}$), 16 Hz (pin $\bar{J}$), 4 Hz (pin Z), and 1 Hz (pin R).

8. Set the load line to a logic "0". This line must be low at the same time the 8 MHz clock is low in order to load the frequency settings. (The Acknowledge line will go low, indicating the data has been loaded).

In order to read the information contained on the programming lines, the following must be performed:

1. Repeat 1, 2, 3 and 4 above.

2. Set the Load line to a logic "1".

3. Set the Read line to a logic "0".

4. Monitor the logic levels on the frequency programming lines (A0 through A21). Lines with a logic "1" indicate that the weight of that line is contributing to the output frequency.

2-4. MODEL 5101 FREQUENCY SYNTHESIZER CHANNEL TIMING INFORMATION

The timing diagram for the Model 5101 channel can be found in Figure 2. Following is a description and specification of these times:

		Min	Max
t_0	Setup time ENABLE to READ	0	-
t_1	Delay time from READ to DATA VALID	-	50 nsec
t_2	Delay time from READ to DATA INVALID	0 nsec	-
t_3	Hold time from ACLK to LOAD	10 nsec	-
t_4	Setup time from LOAD to ACLK	10 nsec	-
t_5	Hold time from ACLK to LOAD	10 nsec	-
t_6	Setup time from LOAD to ACLK	10 nsec	-
t_7	Setup time from DATA VALID to ACLK	30 nsec	-
t_8	Hold time from ACLK to DATA VALID	10 nsec	-
t_9	Setup time from ENABLE to LOAD	10 nsec	-
t_{10}	$\overline{\text{ACLK}}$ pulse width (active low)	50 nsec	75 nsec

NOTES:

1. The A Bus must not be driven by controller whenever ENABLE and READ are active (low).

2. LOAD may be held active (low) for any number of $\overline{\text{ACLK}}$ cycles.

3. Data will be loaded on the low to high transition of $\overline{\text{ACLK}}$ when ENABLE and LOAD are active (low).

4. ENABLE may be used to disable LOAD and READ functions by setting ENABLE high. If ENABLE is tied low, then LOAD and READ will always be enabled.

5101 INTERFACE

PIN	DESCRIPTION	PIN	DESCRIPTION
A	5V GROUND	$\overline{D}$	8 Hz (A18)
B		$\overline{E}$	128 KHz (A4)
C	5V GROUND	$\overline{F}$	64 Hz (A15)
D		$\overline{H}$	32 KHz (A6)
E	HERTZ CARRY (HC)	$\overline{H}$	16 Hz (A17)
F	$\overline{\text{READ}}$	$\overline{K}$	64 KHz (A5)
H	$\overline{\text{ZERO}}$ $\overline{\text{PHASE}}$ ($\overline{\text{ZP}}$)	$\overline{M}$	32 Hz (A16)
J	SIGN BIT (SGN)	$\overline{N}$	$\overline{\text{ENABLE}}$ ($\overline{\text{EN}}$)
K	K HERTZ CARRY (KC)	$\overline{P}$	8 MHz CLOCK ($\overline{\text{ACLK}}$)
L	$\overline{\text{LOAD}}$	$\overline{R}$	
M	2 MHz (A0)	$\overline{S}$	8 MHz CLOCK RETURN ($\overline{\text{CLKR}}$)
N	1 KHz (A11)	$\overline{T}$	+15V
P	2 KHz (A10)	$\overline{U}$	-15V
R	1 Hz (A21)	$\overline{V}$	$\overline{\text{ACKNOWLEDGE}}$ ($\overline{\text{ACKA}}$)
S	1 MHz (A1)	$\overline{W}$	GROUND (±15V)
T	512 Hz (A12)	$\overline{X}$	+15V
U	4 KHz (A9)	$\overline{Y}$	-15V
V	2 Hz (A20)	$\overline{Z}$	$\overline{\text{PRESENCE}}$ ($\overline{\text{PRES}}$)
W	512 KHz (A2)	AA	GROUND (±15V)
X	256 Hz (A13)	BB	
Y	8 KHz (A8)	CC	
Z	4 Hz (A19)	DD	+5V
$\overline{A}$	256 KHz (A3)	EE	
$\overline{B}$	128 Hz (A14)	FF	+5V
$\overline{C}$	16 KHz (A7)	HH	

TABLE 1
Model 5101 Frequency Synthesizer Channel
Remote Interface

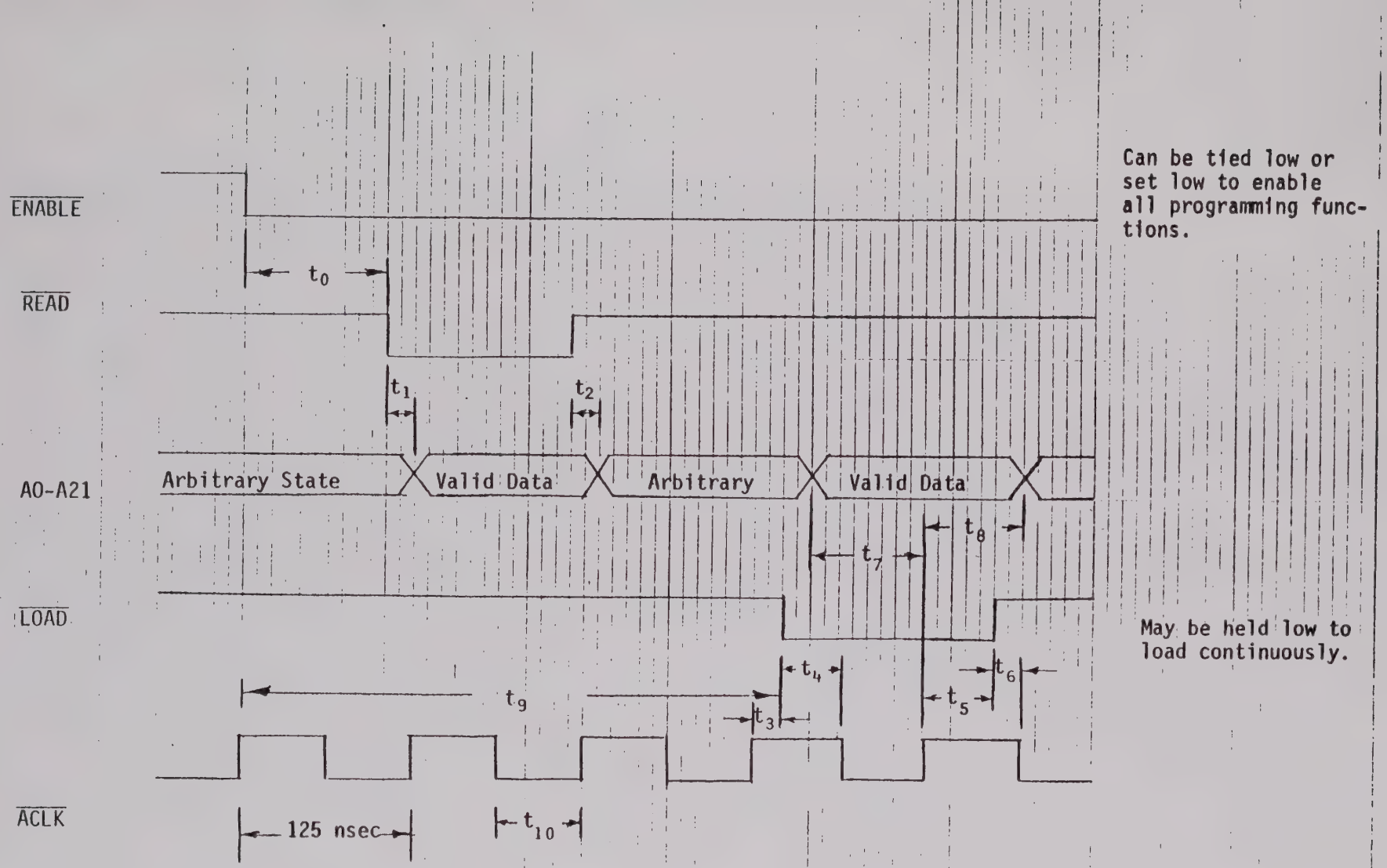


Figure 2
Timing Diagram

SECTION III

SCHEMATICS, ASSEMBLY PRINTS & PARTS LIST

ROCKLAND
Rockland Systems Corporation

TITLE: ASSY MODEL 5101 SYNTHESIZER CHANNEL

LIST OF MATERIAL: 02-004-3161 REV 1

RELEASE AUTHORITY	CHK BY	ENG	MFG	ASSY SIZE	DATE	SHEET
			B.R.	D	7/12/75	2 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
1	0ϕ-320-3161	1	P.C. MAINBOARD (5101)	
2				
3				
4				
5				
6	00-110-1001	7	R: FXD MET FLM 100Ω 1% 1/10W	R58, R56, R54, R52, R44, R42, R40
7	00-110-1691	2	R: 169Ω	R33, R35
8	00-110-2001	2	R: 200Ω	R37, R38
9	00-110-5111	1	R: 511Ω	R36
10	00-110-5621	1	R: 562Ω	R60
11	00-110-7501	1	R: 750Ω	R63
12	00-110-7871	5	R: 787Ω	R28, R29, R30, R31, R32
13	00-110-8251	6	R: 825Ω	R46, R47, R48, R49, R50, R51
14	00-111-1181	1	R: 1.18K	R34
15	00-111-1501	1	R: 1.50K	R41
16	00-111-3091	1	R: 3.09K	R43
17	00-111-6341	1	R: 6.34K	R45
18	00-112-1271	1	R: 12.7K	R53
19	00-112-2551	1	R: 25.5K	R55
20	00-112-4991	1	R: FXD MET FLM 49.9K 1% 1/10W	R57
21				
22				
23	00-116-0101	3	R: FXD COMP 10Ω 5% 1/4W	R11, R10, R39
24	00-116-0301	1	R: 30Ω	R61
25				
26	00-116-0471	4	R: 47Ω	R8, R9, R16, R17
27	00-116-0621	1	R: 62Ω	R25
28	00-116-0821	1	R: 82Ω	R27
29	00-116-1101	2	R: 100Ω	R20, R66
30	00-116-1161	1	R: 160Ω	R1
31	00-116-1181	1	R: 180Ω	R5
32	00-116-1221	2	R: 220Ω	R4, R64
33	00-116-1271	1	R: FXD COMP 270Ω 5% 1/4W	R62

FORM NO 301

ROCKLAND
Rockland Systems Corporation

TITLE ASSY MODEL 5101 SYNTHESIZER CHANNEL

LIST OF MATERIAL 02-004-3161 REV L

RELEASE AUTHORITY | DIR | ENGR JWS | MFG W.R. | ASSY SIZE D | DATE 7/12/75 | SHEET 3 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
34	00-116-1431	1	R: FXD COMP 430Ω 5% 1/4W	R26
35	00-116-1331	1	R: 330Ω	R65
36	00-116-1561	1	R: 560Ω	R15
37	00-116-1821	1	R: 820Ω	R23
38	00-116-2101	6	R: 1.0K	R18, R12, R6, R3, R2, R67
39	00-116-2221	3	R: 2.2K	R22, R19 R14
40	00-116-2751	1	R: 7.5K	R13
41	00-116-4101	1	R: FXD COMP 100K 5% 1/4W	R59
42	00-116-2471	1	R: FXD COMP 4.7K 5% 1/4W	R7
43				
44				
45	00-118-0500	1	R: VAR. CERMET 50Ω 5W	R24
46	00-118-1100	5	R: VAR. CERMET 100Ω 10% 1/2W	R72, R71, R70, R69, R68
47	00-118-2500	1	R: VAR. CERMET 5.0K 10% 3/4W	R21
48				
49				
50				
51				
52	00-100-3101	2	C: FXD CER .01μf +80-20% 30V	C24, C25
53	00-100-4100	14	C: FXD. CER. .1μf +80-20% 15V	C1, C2, C3, C4, C5, C6, C7, C10, C11, C12
54				C13, C35, C33, C34
55	00-101-0510	1	C: FXD. MICA 51pf 10% 500V	C17.
		1	C:	
57	00-101-1180	1	C: FXD MICA 180pf 10% 500V	C21
58	00-101-1820	2	C: FXD MICA 820pf 10% 500V	C18, C20
60	00-109-4100	4	C: FXD TANT .10μf 20% 35V	C16, C28, C29, C22
61	00-109-5100	2	C: TANT 1.0μf 20% 35V	C14, C15
62	00-109-6100	1	C: TANT 10μf 20% 35V	C19
63	00-109-6500	2	C: ELECT 50μf 25V	C26, C27
64	00-109-6680	2	C: FXD TANT 68μf 20% 6V	C8, C9
65	00-106-3470	1	C: FXD CER MLD .047μf 10% 200V	C36
66	00-101-1150	1	C: FXD MICA 150pf 10% 500V	C23

FORM NO 304

ROCKLAND
Rockland Systems Corporation

TITLE: ASSY MODEL 5101 SYNTHESIZER CHANNEL

LIST OF MATERIAL: 02-004-3161 REV L

RELEASE AUTHORITY | CHK'D | ENG | MFG B.P. | ASSY SIZE D | DATE 7/12/75 | SHEET 4 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
67	00-101-2101	1	C: FXD MICA 100 pf 1% 500V	C39
68	00-101-1470	1	C: FXD MICA 470pf 10% 500V	C38
69	00-122-0106	8	U: INT CKT 74195	U4, U6, U8, U13, U20, U24, U27, U31
70	00-122-0131	4	U: 74367	U2, U11, U18, U33
71	00-122-7400	1	U: 7400	U38
72	00-122-7404	1	U: 7404	U54
73	00-122-7410	2	U: 7410	U39, U40
74	00-122-7437	1	U: 7437	U25
75	00-122-7440	2	U: 7440	U16, U45
76	00-122-7474	2	U: 7474	U48, U49
77	00-122-7483	12	U: 7483	U3, U5, U7, U9, U12, U19, U21, U23, U26, U28, U30, U34
78	00-122-9014	7	U: 9014	U15, U22, U29, U36, U41, U42, U43
79	00-123-7474	3	U: 74H74	U14, U35, U37
80	00-124-7474	6	U: 74S74	U50, U51, U52, U53, U55, U56
81	00-125-0109	4	U: INT CKT 74LS174	U1, U10, U17, U32
82	00-129-3000	1	U: ROM 512 X 8 (SIGNETICS)	U44
83	00-120-3529	1	U: VOLT COMP LM361	U46
84	00-120-4830	1	U: DUAL LINE DRIVER 8830	U47
85				
86				
87	00-131-0200	1	CR: SIL ZENER 1N968B	CR6
88	00-131-9622	1	CR: SIL ZENER 1N5234	CR20
89	00-131-9621	1	CR: SIL ZENER 1N962	CR19
90	00-131-9680	2	CR: SIL ZENER 1N754	CR1, CR2
91	00-131-9872	1	CR: SIL ZENER 1N5238 2%	CR21
92	00-132-0457	3	CR: SIL LO LEAK	CR3, CR4, CR5
93	00-133-2800	11	CR: HOT CARRIER	CR8 THRU CR18
94	00-131-9562	1	CR: SIL ZN 5.6V 5% 1W 1N4734A	CR22
95				
96				
97				
98				
99				

FORM NO 304

ROCKLAND
Rockland Systems Corporation

TITLE: ASSY MODEL 5101 SYNTHESIZER CHANNEL

LIST OF MATERIAL: 02-004-3161

REV: L

RELEASE AUTHORITY	CHKD BY	DES	MFG	ASSY SIZE
	DB	MS	O.K.	D

DATE 7/12/75 | SHEET 5 OF 5

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
100	00-134-0065	1 PR	Q: SIL NPN MATCHED PAIR	Q1, Q4
101	00-134-3568	2	Q: SIL NPN 2N3568	Q2, Q5
102	00-134 2222	2	Q: SIL NPN 2N2222	Q17, Q18
103	00-136-4122	11	Q: SIL PNP 2N4122	Q6 THRU Q16
104	00-136-4354	1	Q: SIL PNP 2N4354	Q3
105				
106				
107				
108				
109				
110	00-150-1220	2	L: FXD 220uh ±10%	L3, L4
111	00-150-9151	1	L: FXD 1.5uh ±10%	L1
112	00-150-9220	1	L: FXD 2.2uh ±10%	L2
113				
114				
115				
116	00-165-3002	1	FILTER LOW PASS 0-3MHz	LPF1
117				
118				
119	00-353-1403	2	SOCKET I.C. (14 PIN)	USED ON U25, U49
120	00-353-1604	3	SOCKET I.C. (16 PIN)	USED ON U41, U42, U43
121	00-353-2402	1	SOCKET I.C. (24 PIN)	USED ON U44
122				
123				
124	00-354-0007	15	CONN. TERM. PIN WW.025 (2END)	
125	00-367-0400	2	HEAT SINK TO-8	USED ON Q2, Q3
126	00-368-5001	2	INSULATOR 14 PIN I.C.	USED ON U25, U49
127	00-368-5002	3	INSULATOR 16 PIN I.C.	USED ON U41, U42, U43
128				
129	00.354-0006	5	CONN TERM: .093 X .435	
130	00.378.1761	36"	WIRE # 24 AWG SOLID KYNAR BLUE	
131	00.995.0001	AGF	INK SPEC. DRAWING	
132				

FORM NO 304

LEVEL ,

ROCKLAND
Rockland Systems Corporation

TITLE MODULE CHASSIS 5101 ASSEMBLY

LIST OF MATERIAL 02 002-3161 REV E

RELEASE AUTHORITY | CHK BY PDH | VKS | ASSY SIZE D | DATE 8-29-75 | SHEET 2 OF 3

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
1	02-009-9161	1	CONNECTOR HARNESS ASSY	
2	02-004-3161	1	PWB ASSY CHANNEL 5101	
3	02-002-3161	REF	WIRING DIAGRAM	
4	389.7003	2	CORNER POST MALE	AMP
5	03-002-3161(3SH.)	REF	SCHEMATIC DIAGRAM	
6	.009.0171	1	CABLE ASSY; SHLD RG174 2PT	(17.00)
7	009.0172	1	CABLE ASSY; SHLD RG174 2PT	(7.00)
8	351.0006	2	CONNECTOR, COAX BNC	
9	351.0302	1	CONNECTOR. 3 COND.	
10	171.1600	1	INDICATOR LAMP ASSY LED (DS1)	
11	371.1000	1	LABEL SERIAL NO. TAG	
12	378.4004	12"	CABLE TWISTED 3 COND NO. 24 R/Y/B	
13	377.4001	2	TIE CABLE NYLON CLAMP	
14	378.1961	24"	WIRE NO. 30 AWG	
15	05.706-0600	1	REAR PANEL MODULE 5101	NOTE: ALL HARDWARE TO ASSEMBLE ITEMS 15 THRU 22, 30 & 31 TO BE PROVIDED BY INDUSTRIAL FAB. INC.
16	06.306-0600	REF	ARTWORK REAR PANEL "	
17	05-300-5101	1	FRONT PANEL MODULE 5101	

FORM NO 304

LEV L-3

ROCKLAND
Rockland Systems Corporation

TITLE MODULE CHASSIS 5101 ASSEMBLY

LIST OF MATERIAL 02 | 002-3161

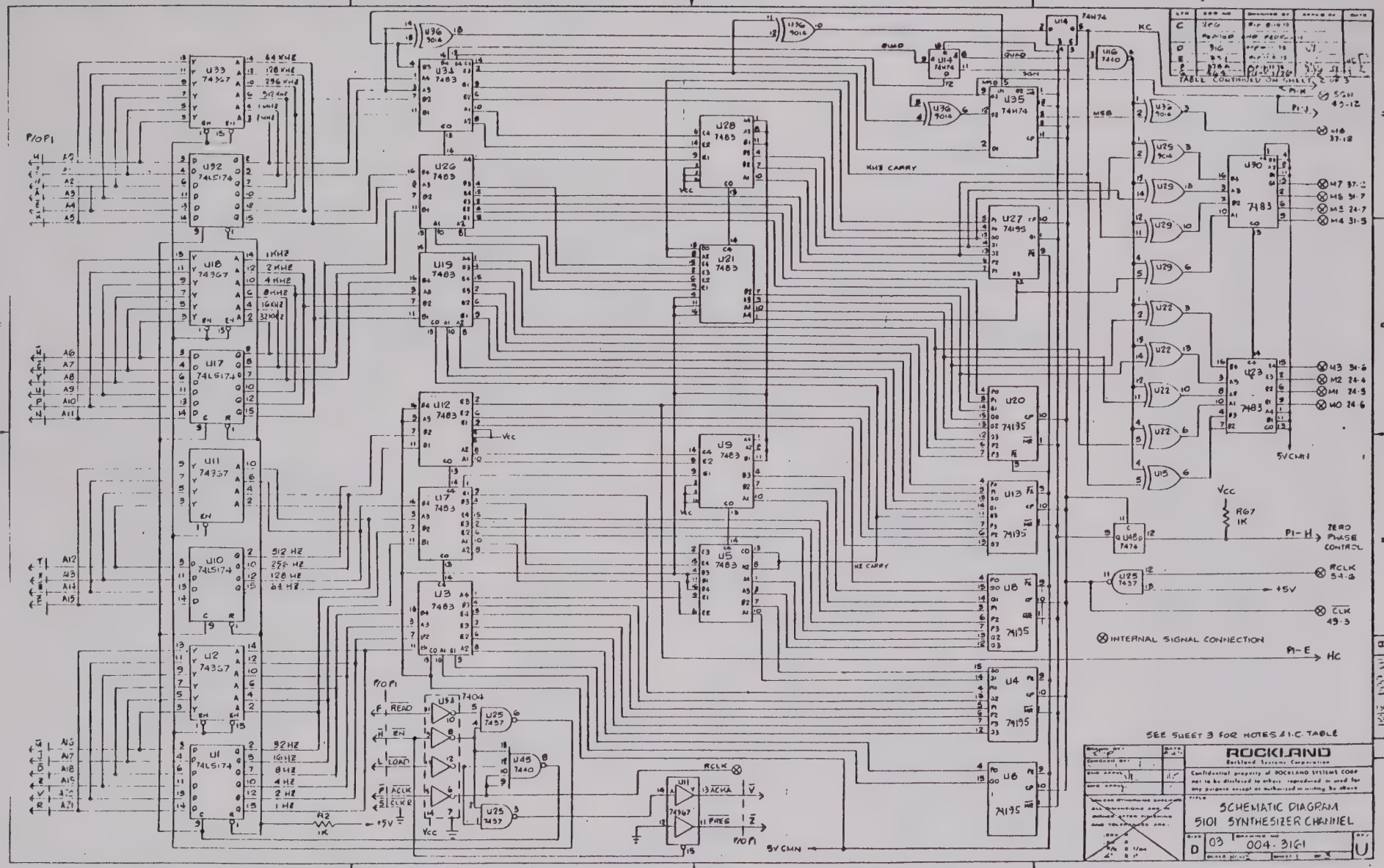
REV E

RELEASE AUTHORITY | CHK BY Rob | | | ADDY SIZE D

DATE 8-29-75 | SHEET 3 OF 3

ITEM	PART NO	QTY	DESCRIPTION	REMARKS
18	06-300-5101	REF	ARTWORK FRONT PANEL 5101	
19	05-306-0902-T	1	MODULE CHSIS RAIL R.H.(TOP)	
20	05-306-0901-T	1	MODULE CHSIS RAIL L.H.(TOP)	
21	05-306-0100	2	MODULE CHSIS PLATE TOP & BOTT	
22	05-306-0500	2	MODULE CHASSIS SIDE PANEL	
23	378.1745	3"	WIRE #24 AWG BOND YELLOW	
24	378.1755	3"	WIRE #24 AWG BOND GREEN	
25	367.6000	1	HOOD, CONNECTOR	
26	380.4041	6	SCREW, MACH. #4-40 B.H. .25LG	
27	388.1041	6	WASHER, LK EXT TOOTH NO.4	
28	388.0040	6	WASHER, FLAT NO.4	
29	387.4060	2	NUT, HEX NO.4-40 SM PATT	
30	05-306.0901-B	1	MODULE CHSIS RAIL L.H(BOTT)	
31	05-306.0902-B	1	MODULE CHSIS. RAIL R.H.(BOTT)	
32	388.1042	2	WASHER, LK SPLIT NO.4	
33	380.4062	2	SCREW, MACH. NO 4-40 P.H. 38 LG	

FORM NO 004

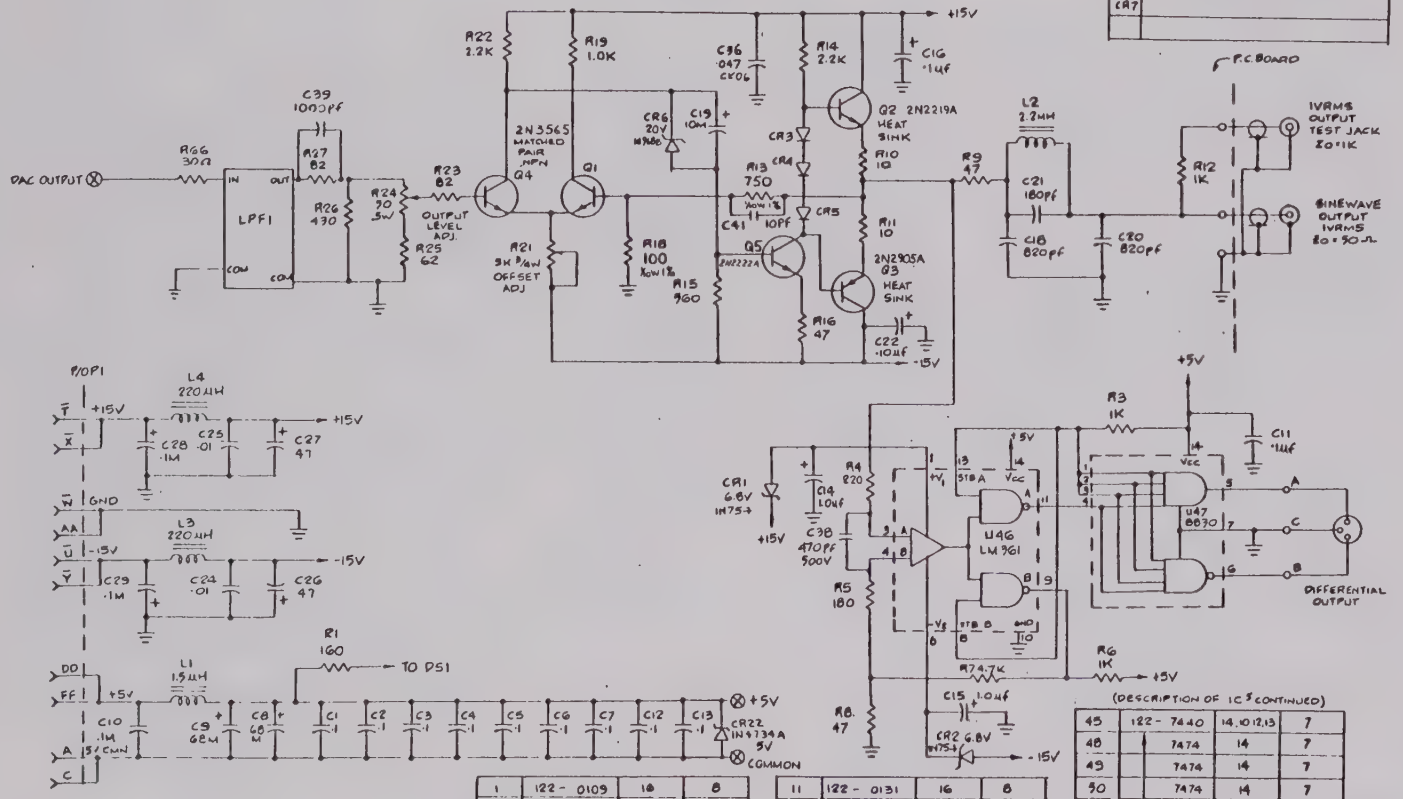

SCHEMATIC DIAGRAM
5101 SYNTHESIZER CHANNEL
ROCKLAND
004-3161
SEE SHEET 3 FOR NOTES & I.C. TABLE
INTERNAL SIGNAL CONNECTION
KHZ CARRY
HZ CARRY
ZERO PHASE CONTROL
+5V
Vcc
SVCMN

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITOR VALUES ARE IN µF.
ALL RESISTOR VALUES ARE OHMS ½W ±5%.

TRANSISTORS ARE TYPE 2N4122.

ALL OTHER COMPONENTS AS SHOWN.
SEE TABLE FOR I.C. DESCRIPTION

REF DESIG NOT USED
CR7



DESCRIPTION OF I.C.'S			
IC NO.	PART NO.	PINS Vcc	PINS GND
3	122-7483	5	12
4	-0106	16	8,9
5	-7453	5	4,11,12,6
6	-0106	16	8,9
7	-7483	5	12
8	-0106	16	8,9
9	-7483	3,5,16	1,8,11,12
12	-7483	4,5	3,12,16
13	-0106	16	8,9
14	-7474	14	7
15	-9014	16	8
16	-7474	14,1,2,4	7
19	-7483	5	12
20	-0106	16	8,9
21	-7483	5	4,11,12,16
22	-9014	16	8
23	-7483	5	1,11,12,13
24	-0106	1,16	8,9
25	-7437	9,14,13	7
26	-7483	5	12
27	-0106	16	8,9
28	-7483	3,5,16	1,8,11,12
29	-9014	16	8
30	-7493	5	1,4,8,11,12
31	-0106	1,16	8,9
34	-7483	5	12
35	-7474	14	7
36	-9014	16	8
37	-7474	14	7
38	-7400	14	7
39	-7410	14	7
40	-7410	14	7
41	-9014	16	5
42	-9014	16	8
43	122-9014	16	8
44	129-9000	24	12,20

1	122-0109	16	8
2	122-0131	16	8
10	122-0109	16	8

11	122-0131	16	8
17	0109	16	8
18	0131	16	8
92	0109	16	8
33	122-0131	16	8
46	LM361	14	10
47	8830	14	7

(DESCRIPTION OF I.C.'S CONTINUED)

45	122-7440	14,10,12,13	7
48	7474	14	7
49	7474	14	7
50	7474	14	7
51	7474	14	7
52	7474	14	7
53	7474	14	7
55	7474	14	7
56	122-7474	14	7
54	122-7404	14	7

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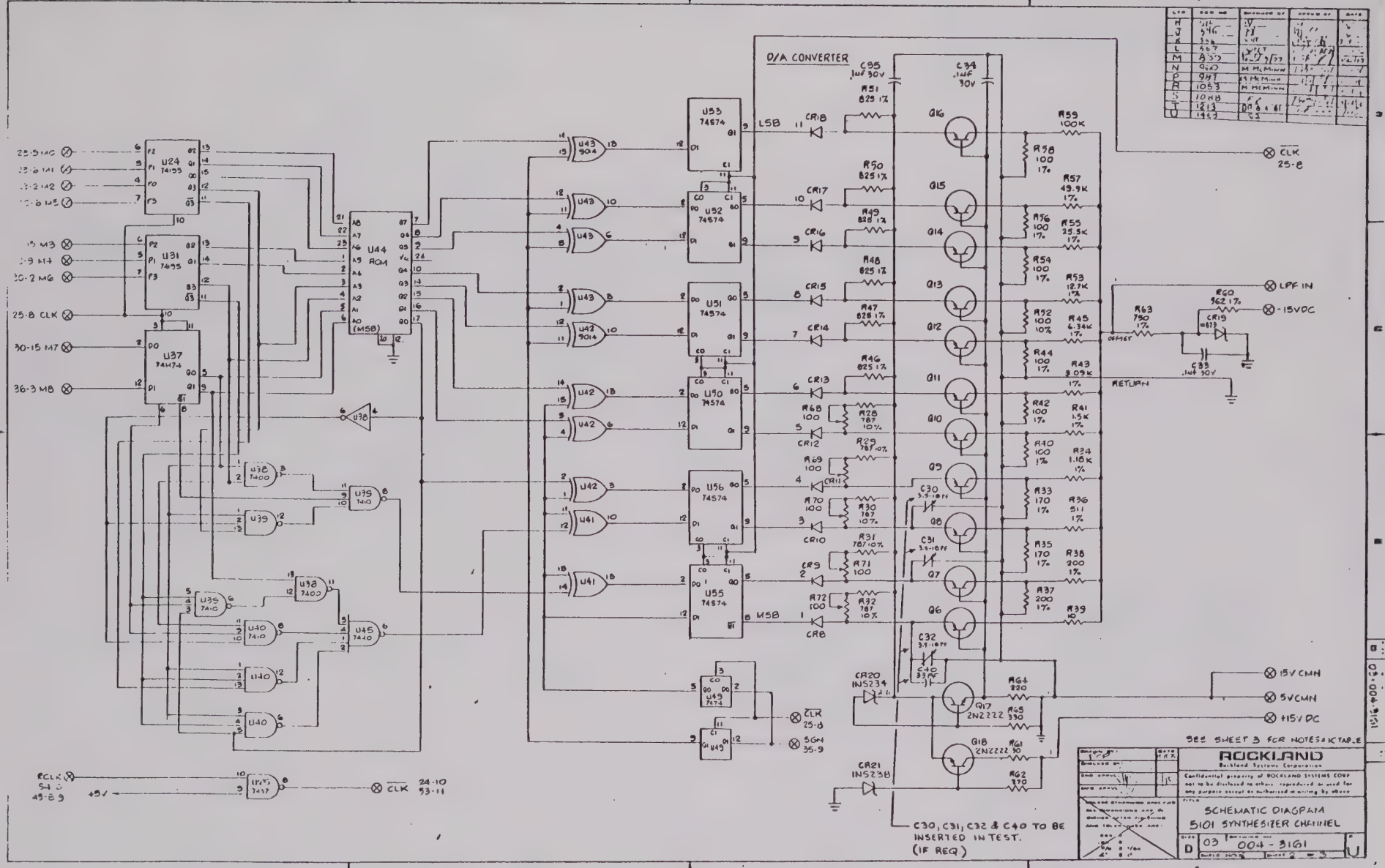
SCHEMATIC DIAGRAM
5101 SYNTHESIZER CHANNEL

D 03 004-3161 U


D/A CONVERTER
C35 .1uF 30V
C34 .1uF 30V
U24 74155
U31 74155
U37 74H74
U44 ROM (MSB)
U43 9014
U42 9014
U53 74S74
U52 74S74
U51 74S74
U50 74S74
U56 74S74
U55 74S74
U49 7474
U38 7400
U39 7410
U35 7410
U40 7410
U45 7410
U36 7404
LSB
MSB
CR18
CR17
CR16
CR15
CR14
CR13
CR12
CR11
CR10
CR9
CR8
R51 825 1%
R50 825 1%
R49 828 1%
R48 825 1%
R47 828 1%
R46 825 1%
R28 787 1%
R29 787 1%
R30 787 1%
R31 787 1%
R68 100
R69 100
R70 100
R71 100
R72 100
R32 787 1%
Q16
Q15
Q14
Q13
Q12
Q11
Q10
Q9
Q8
Q7
Q6
R59 100K
R58 100 1%
R57 49.9K 1%
R56 100 1%
R55 25.5K 1%
R54 100 1%
R53 12.7K 1%
R52 100 1%
R45 6.34K 1%
R44 100 1%
R43 3.09K 1%
R42 100 1%
R41 1.5K 1%
R40 100 1%
R34 1.18K 1%
R33 170 1%
R36 511 1%
R35 170 1%
R38 200 1%
R37 200 1%
R39 10
R63 750 1%
R60 562 1%
CR19 HP5082-2811
C33 .1uF 30V
OFFSET
RETURN
C30 3.5-18pF
C31 3.5-18pF
C32 3.5-18pF
C40 33pF
CR20 IN5234
CR21 IN5238
Q17 2N2222
Q18 2N2222
RG4 220
RG5 330
RG1 10
RG2 330
CLR 25-8
SGN 35-9
LPF IN
-15VDC
15V CMN
5V CMN
+15V DC
RCLK
+5V
CLK 24-10 53-11
SEE SHEET 3 FOR NOTES & TABLE
C30, C31, C32 & C40 TO BE INSERTED IN TEST. (IF REQ.)
ROCKLAND
Rockland Systems Corporation
SCHEMATIC DIAGRAM
5101 SYNTHESIZER CHANNEL
D 03 004-3161

LTR	ECO NO.	CHANGED BY	APPV'D BY	DATE
A	RELEASE	Rep 12-23-75		

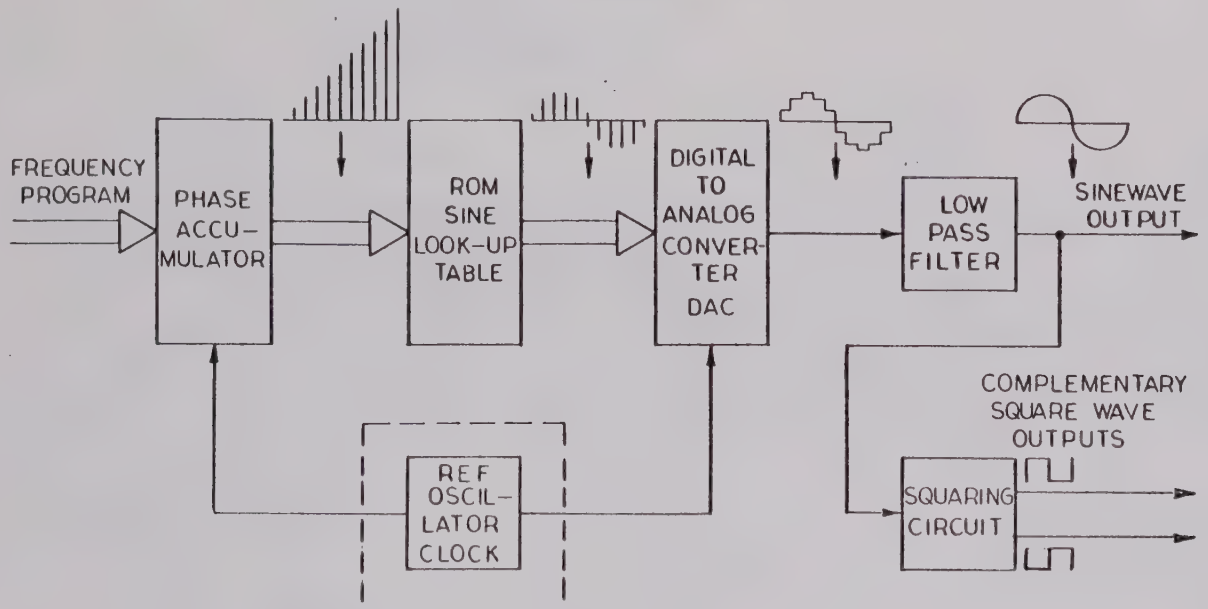


FIG. 4-1

DRAWN BY: PSh	DATE 10-9-74	ROCKLAND Rockland Systems Corporation
CHECKED BY:		
ENG APPVL. PHH	10-10-74	Confidential property of ROCKLAND SYSTEMS CORP. not to be disclosed to others, reproduced or used for any purpose except as authorized in writing by above.
MFG APPVL.	12-23	

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE:
.XXX ±
.XX ±
X/x ± 1/64
∠° ± 1°

TITLE: FUNCTIONAL BLOCK DIAGRAM MODEL 5101 SYNTHESIZER CHANNEL

SIZE	DRAWING NO	REV
B	04 004.3161	A

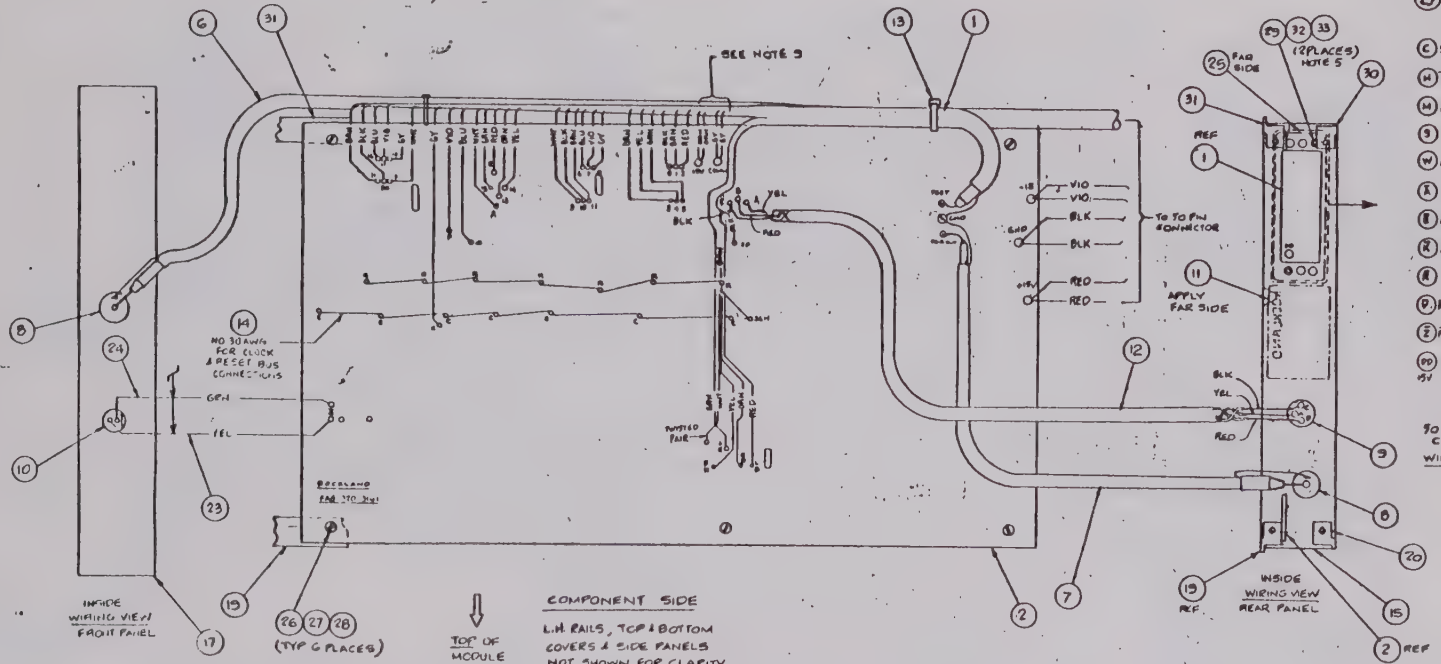
SCALE ~ SHEET 1 OF 1

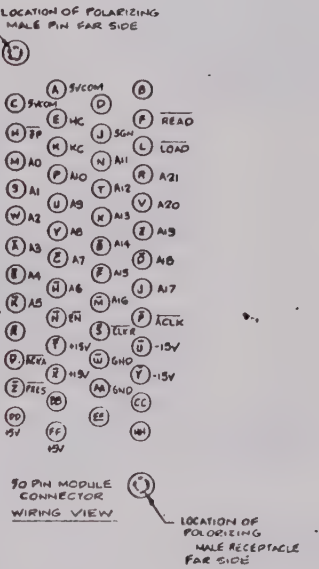
SIZE B DWG NO 04.004.3161 REV A

NOTES:

1. ASSEMBLE ITEM 1 TO 2. DO NOT PLUG IN 18V SUPPLY WIRES.
2. MOUNT ITEMS 8 & 9 TO ITEM 18.
3. MOUNT ITEM 30 TO ITEM 18.
4. ASSEMBLE ITEM 2 TO ITEMS 19 & 31.
5. INSERT ITEM 1 THRU HOLE IN ITEM 19 & INSTALL HOOD ITEM 28. MOUNT ITEM 31 TO ITEM 19. INSTALL HARDWARE ITEMS 32, 33 & 29, ALIGN USING RODS & TIGHTEN HARDWARE.
6. MOUNT ITEM 20 TO ITEM 18.
7. MOUNT ITEMS 8 & 10 TO ITEM 17.
8. MOUNT ITEM 17 TO ITEMS 19, 20, 30 & 31.
9. WIRE ITEMS 6, 7, 12, 23 & 24 PER ASSY PICTURE PLUG IN 18V SUPPLY & GND WIRES
10. MOUNT ITEM 11 TO ITEM 19.

LTR	ECO NO	DESCRIPTION OF CHANGE	APPROVED BY	DATE
A	PRELIMINARY			
B	383			
C	398			
D	960			
E	878A			





SHEETS 2 & 3 'A' SIZE P/L

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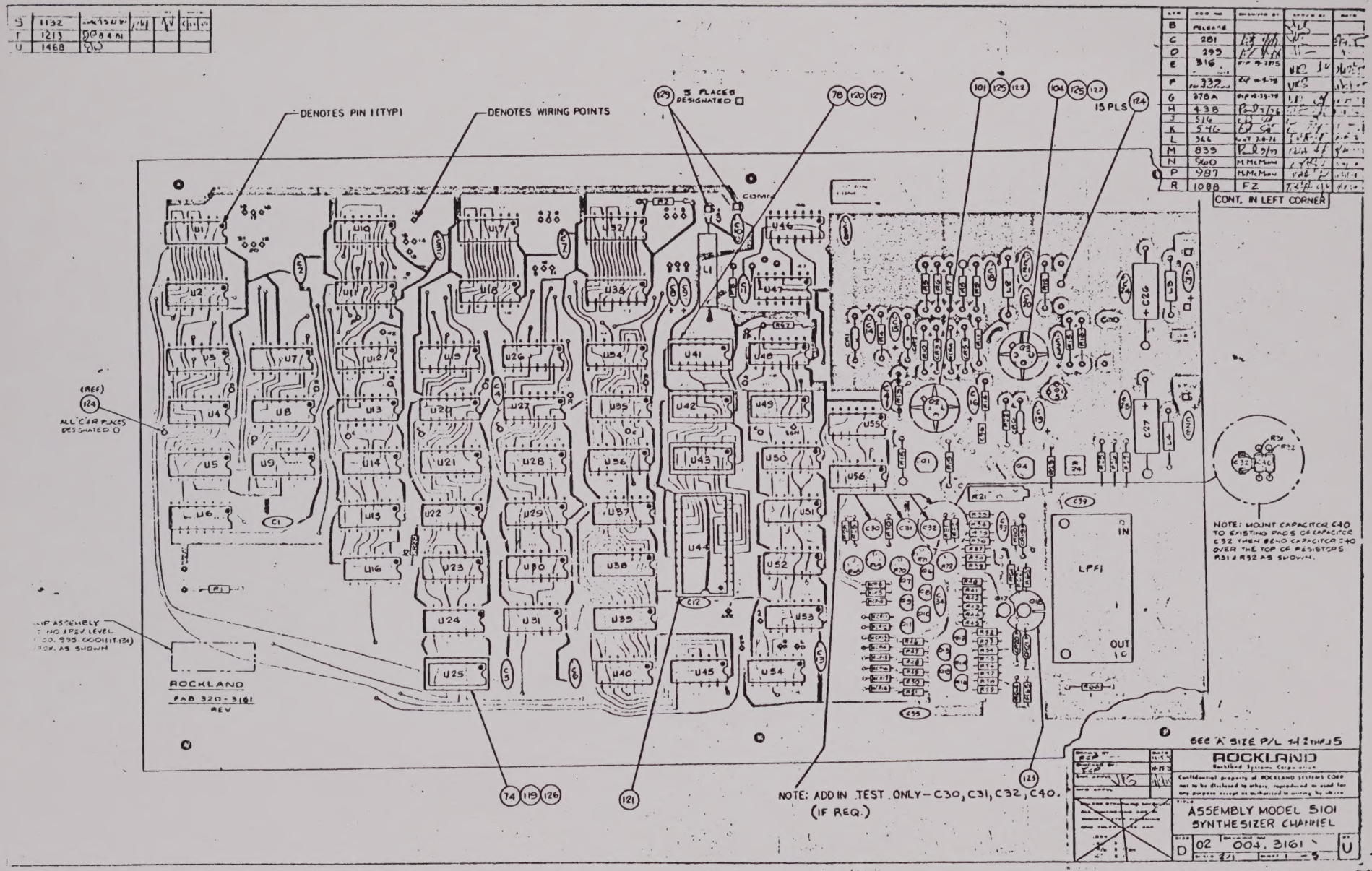
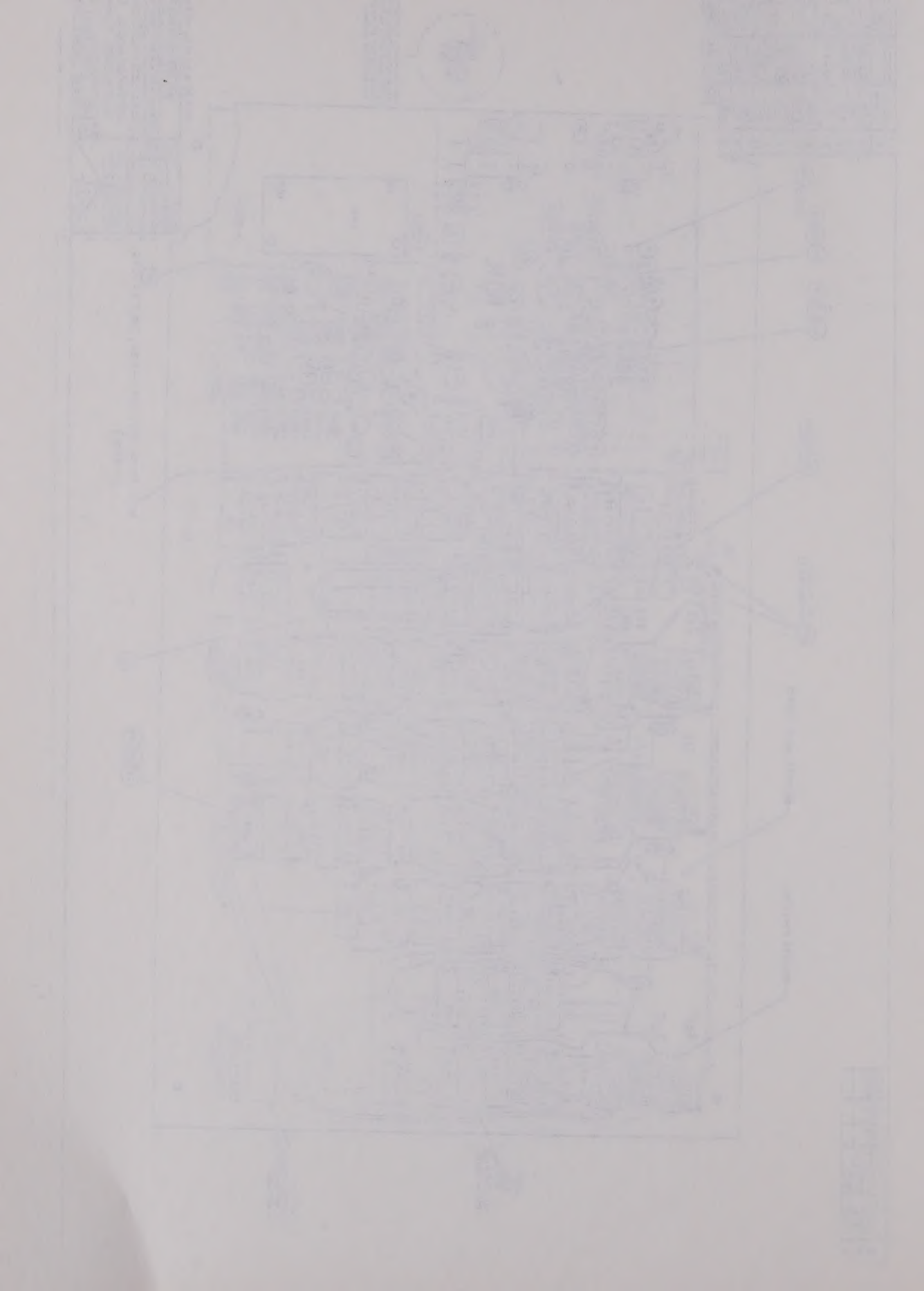
MODULE CHASSIS 3101
(WIRING DIAGRAM ASSY)

D | 02 | 002-3161 | E


DENOTES PIN 1 (TYP)
DENOTES WIRING POINTS
3 PLACES DESIGNATED
15 PLS
CONT. IN LEFT CORNER
ALL CAP PLACES DESIGNATED C
NOTE: MOUNT CAPACITOR C40 TO EXISTING PADS OF CAPACITOR C32 THEN BEND CAPACITOR C40 OVER THE TOP OF RESISTORS R31 & R32 AS SHOWN.
NOTE: ADD IN TEST ONLY – C30, C31, C32, C40. (IF REQ.)
SEE 'A' SIZE P/L SH 2 THRU 5
ROCKLAND
FAB 320-3161
REV
LPF1
IN
OUT
ASSEMBLY MODEL 5101 SYNTHESIZER CHANNEL
D 02 004.3161 U



MP MASTER
MA35651